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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/588,769	05/07/2007	Tadahiro Kuroda	060570	4675

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EXAMINER	
SEMENENKO, YURIY	
ART UNIT	PAPER NUMBER
2841	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/588,769	KURODA ET AL.	
	Examiner	Art Unit	
	YURIY SEMENENKO	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *08/08/2006; 09/15/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Preliminary amendment filed on 08/08/2006 has been entered.
Claims 6-7 are newly added.
Claims 1-7 are now pending in the application.

Claim Objections

2. Claim 1 is objected to because of the following informalities:
claim 1,line 2: "a substrate" should be changed to – the first substrate—for proper antecedence basis.
claim 1,line 3: "a substrate" should be changed to – the second substrate—for proper antecedence basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Onizuka et al., (The Fundamentals and Frontiers 2003 Conference of Nen The Institute of Electronics,

Information and Communications Engineers Kiso Kyokai Society Taikai Koen Ronbunshu; Japan, 09/18/2003) hereinafter Onizuka.

Regarding claim 1: Onizuka discloses in Fig. 1 discloses an electronic circuit according to the invention comprising: a first substrate (substrate of the Chip 1, fig. 1) including a first coil L_1 that is formed by wiring on a substrate (lines are shown in fig. 1); and a second substrate (substrate of the Chip 2) including a second coil L2 that is formed by wiring on a substrate at a position corresponding to said first coil (shown in fig. 1), and is inductively coupled to said first coil.
Instant Onizuka clearly teaches all of the applicant's claimed invention. However, the examiner notes that limitation "to form coils by wiring on a substrate" is within of the common knowledge of person of ordinary skill in the art. Further, a limitation "is formed by wiring" is a process limitation in the product claim. Such process limitations define the claimed invention over the prior art only to the degree that they define the product itself. A process limitation cannot serve to patentably distinguish the product over the prior art, in the case that the product is the same as, or obvious over, the prior art. See Product-by-Process in MPEP 2113 and 2173.05(p) and In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 2- 7 are rejected under 35U.S.C. 103(a) as being unpatentable over Onizuka as applied to claim 1 above, and further in view of Weber et al., (US 5701037) hereinafter Weber.

Regarding claim 2: Onizuka discloses the electronic circuit having all of the claimed features as discussed above with respect to claim 1,

except, Onizuka doesn't explicitly teach said first substrate further includes a transmitter circuit for outputting signals to said first coil when transmission digital data changes.

Weber teaches in fig. 3 a transmitter circuit S for outputting signals to the coil SP_s when transmission digital data changes.

Therefore it would have been obvious to one of ordinary skill in the art, at the time the invention was made for Onizuka to include in his invention said first substrate further includes a transmitter circuit for outputting signals to said first coil when transmission digital data changes, as taught by Weber because Weber teaches the signal transmission would function reliably even if, surface ripple of the chip layers and irregularities of the interlayer dielectric modify the coil spacing and, thus, the coupling inductance, (col. 2:20-23).

Regarding claims 3 and 6: Onizuka discloses the electronic circuit having all of the claimed features as discussed above with respect to claim 1(2), wherein said second substrate (substrate of the Chip 2, fig. 1) further includes a receiver circuit (shown in fig. 1) that connects both ends of said second coil L_2,

except, Onizuka doesn't teach a receiver circuit that connects both ends of said second coil to a predetermined voltage source via resistors.

Although Weber teaches in fig. 7 the receiver circuit that connects only one end of the resistors R_1 to a predetermined voltage source, the prior art structure (discloses resistors R_1 and R_2 connected to a predetermined voltage source) is capable of performing the intended use (connects both ends of said second coil to a predetermined voltage source via resistors), then it meets the claim. See In re Casey, 152 USPQ 235 (CCPA 1967) and In re Otto, 136 USPQ 458, 459 (CCPA 1963).

Therefore it would have been obvious to one of ordinary skill in the art, at the time the invention was made for Onizuka to include in his invention said second substrate further includes a receiver circuit that connects both ends of said second coil to a predetermined voltage source via resistors, as taught by Weber in order to provide voltage variation a receiver circuit.

Regarding claim 4: Onizuka discloses the electronic circuit having all of the claimed features as discussed above with respect to claim 1, wherein said first coil L_1, fig. 1 is inductively coupled to said second coil L_2,

except, Onizuka doesn't teach a plurality of said second substrate.

Weber teaches the coils L_2 on each of the plurality of the stacked chip layers (col. 3;18-19). Further, In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960) (Although the reference did not disclose a plurality of ribs, the court held that mere duplication of parts has no patentable significance unless a new and unexpected result is produced.).

Therefore it would have been obvious to one of ordinary skill in the art, at the time the invention was made for Onizuka to include in his invention a plurality of said second substrate, as taught by Weber in order to provide multi-layers electronic devices

and since the court held that mere duplication of parts has no patentable significance unless a new and unexpected result is produced.) In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960).

Regarding claims 5 and 7: Onizuka discloses the electronic circuit having all of the claimed features as discussed above with respect to claim 1(2), wherein said second substrate (substrate of the Chip 2, fig. 1) further includes a receiver circuit (shown in fig. 1) that receives signals,

except Onizuka doesn't teach a receiver circuit that receives signals only for a predetermined cyclic period.

Weber teaches in fig. 3-7 a receiver circuit that receives signals only for a predetermined cyclic period, fig. 2. further the prior art structure is capable of performing the intended use, then it meets the claim. See In re Casey, 152 USPQ 235 (CCPA 1967) and In re Otto, 136 USPQ 458, 459 (CCPA 1963).

Therefore it would have been obvious to one of ordinary skill in the art, at the time the invention was made for Onizuka to include in his invention a receiver circuit that receives signals only for a predetermined cyclic period, as taught by Weber in order to receive transmission data.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Dupuis – US 7460604;

Haigh et al. – US 6903578;

Sakurai et al. – PG Pub. No. 2006/0038544.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yuriy Semenenko whose telephone number is (571) 272-6106. The examiner can normally be reached on 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean A. Reichard can be reached on (571)- 272-2800 ext. 31. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Y. S./
Examiner, Art Unit 2841

/Dean A. Reichard/
Supervisory Patent Examiner, Art Unit 2841